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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
NGUYEN, CUONG QUANG

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/595,860	Applicant(s) BERTHOLD ET AL.	
	Examiner Cuong Q Nguyen	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23 and 25-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23 and 25-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-9, 17-23, 25-26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheek et al. (US 5,935,766) in view of Chiang et al. (US 5,739,579).

Regarding claims 1, 3- 6, 14, 15, 16, Cheek et al. discloses an integrated circuit comprising: a plurality of structure planes on which the metalizations are formed; the structure planes including an element structure plane (a substrate 100); electrically active elements formed on the element structure plane; an insulation layer (130, a semiconductor oxide layer. Col.6 lines 12-19) formed above the element structure plane; electrical connecting leads (copper contact pads 220, 222, 224. Col.10, lines 5-9) formed above the insulation layer; connection pieces (Al metal-1 layers 150, 152, 154. Col.6, lines 35-40) formed underneath the electrical connecting leads and covering the contact holes (140, 142, 144) in the insulating layer; the connection pieces are covered by isolation layer (160); a plurality of further contact holes (180, 182, 184)

formed in the isolation layer and are filled with metal (190, 192, 194), wherein metal is connected to at leat one of connecting leads. See Cheek et al.'s Fig.1N.

Cheek et al. does not teach that diffusion blocker layers formed between each of a plurality of structure planes, wherein the diffusion blocker is interrupted only in a region having contact holes and the connection pieces covering the contact hole.

Chiang et al. discloses an integrated circuit comprising: silicon nitride diffusion blocker layers (323, 390, 392) having a thickness in the range of 30 nm to 150 nm (Chiang et al.'s col.15, lines 17-22) formed between each of a plurality of structure planes, wherein the diffusion blocker layer is interrupted only in a region having contact holes and the connection pieces covering the contact hole. See Chiang et al.'s Fig.25.

It would havbe been obvious to one of ordinary skill in the art to incorporate the silicon nitride blocker layers between the structure planes as taught by Chiang et al. into Cheek et al.'s device in order to prevent electrical shorting. Chiang et al..'s col.15, lines 4-15.

It is noted that the diffusion blocker of above combination formed of silicon nitride is that the same material the diffusion blocker in the present invention. Therefore, it is inherent that the diffusion blocker in the device formed by the combination of Cheek et al. and Chiang et al. has capability of preventing a diffusion of copper as claimed.

Regarding claim 2, Cheek et al. teaches that diffusion barriers of Ti/TiN for impeding a diffusion of copper formed on a surface of contact holes. Cheek et al.'s col.6, lines 20-30.

Regarding claim 7, Chiang et al. does not explicitly teach that silicon nitride bloker is a Si3N4.

It would have been obvious to one of ordinary skill in the art to form the blocker layer of Si3N4 as claimed because silicon nitride is commonly Si3N4.

Regarding claims 8, 9, Chiang et al. teaches that the blocker layers formed of SiON. See Chiang et al.'s col.14, lines 65-67.

Regarding claims 18, 19, 20, Cheek et al. does not teach that the further blocker layer formed on the top and side areas of copper electrical connecting leads to prevent the bulk outdiffusion of copper into the insulation layer.

Chiang et al. teaches that a further blocker layer (121) formed on the top and side areas of copper connecting leads (120) to prevent bulk outdiffusion of copper into the insulation layer (122). See Chiang et al.'s Fig.12.

It would have been obvious to one of ordinary skill in the art to incorportae the further blocker layer over the copper connecting lead as taught by Chiang et al. into Cheek's device in order to prevent bulk outdiffusion of copper into the insulation layer. See Chiang et al.'s col.2, lines 50-58.

Regarding claims 17 and 21-23, Chiang et al. does not teach that the blocker layer (23) has a thickness greater than a thickness of the further blocker (121) so that. a diffusion through the blocker layer is less than 10% of a diffusion through the further diffusion blocker.

It is known in the art that the diffusion through the blocker layer is depending on the thickness of the blocker.

Therefore, it would have been obvious to one of ordinary skill in the art to form the blocker layer having a thickness greater than the thickness of further blocker layer so that the diffusion through the blocker layer is less than 10% of a diffusion through the further diffusion blocker as claimed because the thickness of blocker layers are art recognized variable of importance which are subject to routine experimentation and optimization.

Regarding claim 25, Check et al. teaches that the metal filling the contact holes is tungsten. Cheek et al.'s col.6, lines 25-30.

Regarding claim 26, Cheek et al. does not teach that the metal filling the contact holes is copper.

Chiang et al. teaches that the metal filling the contact hole (342) could be tungsten or copper. See Chiang et al.'s Fig.25 and col.14 lines 1-3.

It would have been obvious to one of ordinary skill in the art to fill the contact hole with copper instead of tungsten as taught by Chiang et al. because tungsten and copper are art recognized material for filling the contact holes in the semiconductor integrated circuit.

Regarding claim 28, the further blocker on top and side surface of the connection pieces is considered as the blocker layer so that an upper surface of the blocker layer facing the structure plane and connection pieces are incontact with a lower surface of the blocker layer.

Claims 1-7, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheek et al. (US 5,935,766) in view of Bothra et al. (US 5,798,559).

Regarding claims 1, 3- 6, Cheek et al. discloses an integrated circuit comprising: a plurality of structure planes on which the metalizations are formed; the structure planes including an element structure plane (a substrate 100); electrically active elements formed on the element structure plane; an insulation layer (130, a semiconductor oxide layer. Col.6 lines 12-19) formed above the element structure plane; electrical connecting leads (copper contact pads 220, 222, 224. Col.10, lines 5-9) formed above the insulation layer; connection pieces (Al metal-1 layers 150, 152, 154. Col.6, lines 35-40) formed underneath the electrical connecting leads and covering the contact holes (140, 142, 144) in the insulating layer; the connection pieces are covered by isolation layer (160); a plurality of further contact holes (180, 182, 184)

formed in the isolation layer and are filled with metal (190, 192, 194), wherein metal is connected to at leat one of connecting leads. See Cheek et al.'s Fig.1N.

Cheek et al. does not teach that diffusion blocker layers formed between each of a plurality of structure planes, wherein the diffusion blocker is interrupted only in a region having contact holes and the connection pieces covering the contact hole.

Bothra et al. discloses an integrated circuit comprising: silicon nitride diffusion blocker layer (116) formed between the element structure plane (a substrate 100) and insulation layer (106), wherein the diffusion blocker layer is interrupted only a region having contact holes and the connection pieces covering the contact hole. See Bothra et al.'s Fig.3K.

It would havbe been obvious to one of ordinary skill in the art to incorporate the silicon nitride blocker layers between between the element structure plane and insulation layer as taught by Bothra et al. into Cheek et al.'s device in order to protect the substrate from corrosion and contaminants. Bothra et al.'s col.4, lines 52-58.

It is noted that the diffusion blocker formed of silicon nitride the same material the diffusion blocker in the present invention. Therefore, it is inherent that the diffusion blocker in the device formed by the combination of Cheek et al. and Bothra et al. has capability of preventing a diffusion of copper as claimed.

Regarding claim 2, Cheek et al. teaches that diffusion barriers of Ti/TiN for impeding a diffusion of copper formed on a surface of contact holes. Cheek et al.'s col.6, lines 20-30.

Regarding claim 7, Bothra et al. does not explicitly teach that silicon nitride bloker is a Si3N4.

It would have been obvious to one of ordinary skill in the art to form the blocker layer of Si3N4 as claimed because it is known in the art that silicon nitride is commonly expressed as Si3N4.

Regarding claim 27, the limitation " the blocker layer includes an upper surface facing said isolation layer and a lower surface facing said structure plane, said connection pieces being in contact with said upper surface of said blocker layer " is flown naturally in the device formed by the combination of Cheek et al. and Bothra et al.

Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheek et al. in view of Chiang et al. and further in view of Hong (US 6,008,117).

Cheek et al. and Chiang et al. substantially teach all the limitations of claims 1-9, 17-23, 25-26 and 28 as shown above but fail to teach that the blocker layer is formed of metal oxide such as TiO2.

Hong discloses an integrated circuit comprising a blocker layer (14) is formed of silicon nitride or TiO2. See Hong's Fig.1H and col.2 lines 52-56.

It would have been obvious to one of ordinary skill in the art to form the blocker layer of TiO2 instead of silicon nitride as taught by Hong because materials such as silicon nitride,and TiO2 are art recognized materials for forming the blocker layer in the semiconductor device and they are interchangeable.

Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheek et al. in view of Chiang et al. and further in view of McCollum et al. (US 5,552,627).

Cheek et al., Chiang et al. teach all the limitations of claims 1-9, 17-23, 25-26 and 28 as shown above but fail to teach that the blocker layer is formed of a fluorinated nitride such as fluorooxynitride.

McCollum et al. discloses an integrated circuit comprising a blocker layer formed of fluorinated nitride material by deposited the silicon nitride using an NF3 atmosphere in the reactor. McCollum et al. teaches that fluorinated nitride has a lower leakage than a similar nitride material. See McCollum et al.'s Fig.3 and col.8, lines 42-51.

Therefore, it would have been obvious to one of ordinary skill in the art to form the block layer of silicon nitride or silicon oxynitride by deposited the silicon nitride using an NF3 atmosphere as taught by McCollum et al. in order to reduce the leakage of the blocker layer.

It is inherent that the silicon oxynitride is formed by deposited the silicon nitride using an NF3 atmosphere would produce fluorinated nitride such as fluorooxynitride.

Response to Arguments

2. Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

4. Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG

30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

5. Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to CUONG Q NGUYEN whose telephone number is (703) 308-1293. The Examiner is in the Office generally between the hours of 6:30 AM to 5:00 PM (Eastern Standard Time) Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor TOM THOMAS who can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7722 or 308-7724.

Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center Receptionists whose telephone number is 308-0956.

CN

March 20, 2002

Tom Thomas

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